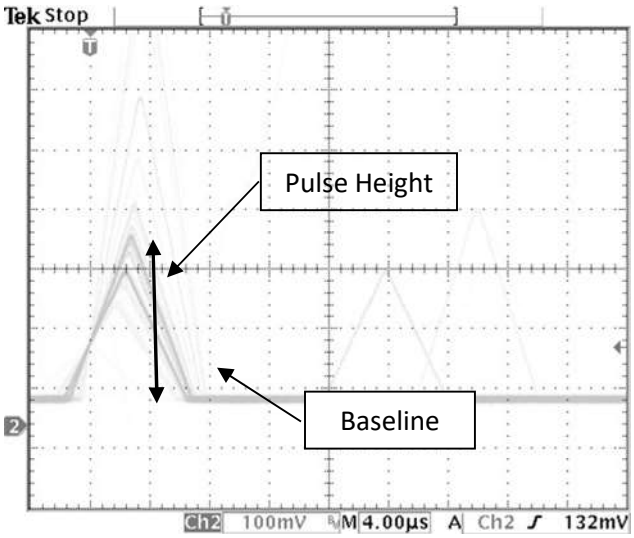
Baseline Restorer Mode 3

What is the "baseline restorer"?

The digital pulse processor (DPP) produces a pulse for each X-ray interacting in the detector. The plot to the right shows measured typical pulses. The amplitude of the pulse, above the baseline, is related to the energy deposited. The system measures the peak amplitude with great accuracy, but it is the amplitude above the baseline which is critical.



One might assume that the baseline is zero, but in real systems it differs from zero for various reasons (offset voltages are non-zero, etc.). It can shift up and down, causing changes in the measured pulse amplitudes. This shows up in the spectrum as a shift in all the peak channels, which can lead to errors in spectroscopy. The baseline typically shifts with count rate (a consequence of AC coupling in the signal processing), with temperature, and possibly with other effects. The baseline restorer (BLR) monitors the baseline, detects any errors, and then produces a correction signal to keep the baseline stable. It is a specific feedback loop.

What is the difference between BLR Mode 1 and BLR Mode 3?

Amptek's BLR Mode 1 is an asymmetric baseline restorer. It uses the fact that signal pulses are unipolar, positive going, so any negative going fluctuations arise from noise. It monitors the maximum negative going deviation and keeps this at a fixed channel; if the rms noise is constant, the baseline will be constant. The BLR Mode 1 uses only information in the slow channel to stabilize it.

Amptek's BLR Mode 3 is a gated, symmetric baseline restorer. As a symmetric restorer, it implements a weighted average of the signal between pulses, using both the positive and negative going fluctuations. It is gated off during pulses, so that it only measures noise. It uses the signal in the fast channel to detect the presence of a pulse and to gate off the slow channel BLR logic.

What are the advantages and disadvantages of the two modes?

Amptek's DPPs have used Mode 1 for many years. It is quite simple to use and operates quite well under most circumstances. Because it uses only the slow channel to determine the slow channel baseline, it is relatively simple and robust. But at sufficiently high dead times, it does not correct enough and the baseline drifts.

BLR Mode 3 is a new development. It works better than Mode 1 at the highest rates, better stabilizing the baseline, which also improves energy resolution. The plots below illustrate the improvement under typical conditions. Its disadvantage is some additional complexity in tuning it correctly: because it relies on the fast channel, the fast channel's parameters are critical. In addition, the fast channel peaking time must be much shorter than the slow channel peaking time. At the shortest peaking times, the slow channel is not much slower than the fast channel, and Mode 3 does not work as well as Mode 1.

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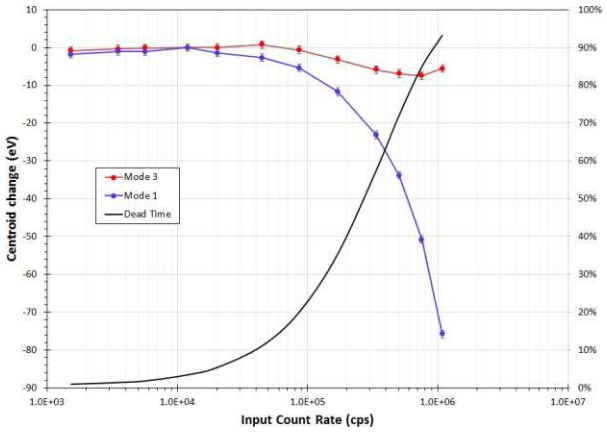

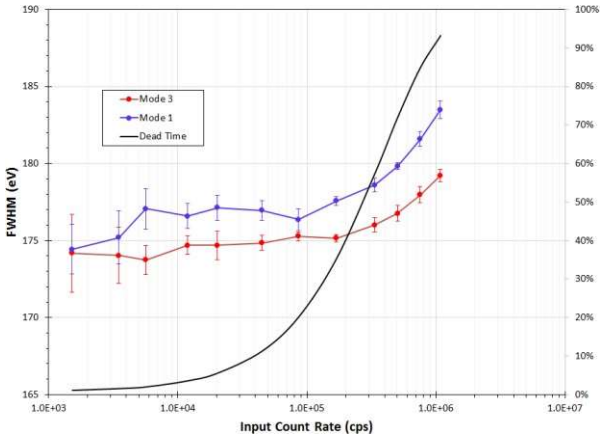

For most users, we recommend retaining Mode 1 as a simple, robust, and good algorithm. For peaking times below 0.5 μs, we recommend Mode 1. For users operating at peaking times above 0.5 μs, at the highest count rates and dead times, and with the tightest stability requirements, we recommend using Mode 3.

How do I optimally configure using Mode 1?

The BLR settings are located in the "Shaping" tab of DPPMCA. First, set the BLR Mode to 1. Second, you need to choose "UP" and "DN" settings. These control the slew rate of the BLR feedback signal. If the BLR detects a baseline shift, using a higher value for UP or DN will give a faster slew and thus faster recovery but this can also degrade resolution. Amptek typically uses UP of 0, DN of 3 as a good, general setting. Higher count rates may give better results with 2, 2. The user can experiment to find the best in his/her application.

How do I optimally configure using Mode 3?

- BLR Mode 3 is available for the DP5 and DP5-X. It is not available for the PX5.
- To use Mode 3, one must first install a recent version of the DPPMCA software (ver 1.0.0.22 or later) and of the DP5 firmware (FW 6.09.09 and FP 7.03 or later). Firmware can be installed using Firmware Manager, (available at the bottom of the page at this link https://www.amptek.com/software/dp5-digital-pulse-processor-software) Note that BLR Mode 3 and List Mode are not both supported in a single FPGA version. An FPGA version must be chosen that supports one or the other feature, as there isn't room in the FPGA for both features.
- Set the BLR Mode to 3. This is the only parameter that is critical for the slow channel.
- Make sure the fast channel is much faster than the slow channel. Make sure the fast channel threshold is set correctly (this is discussed in the DPPMCA "Help topics".