Charge Sensitive Preamplifier A250

STATE-OF-THE-ART

- **External FET allows matching to detector**
- **FET can be cooled**
- **Noise at room temperature ~ 100 electrons RMS**
- **Low power (19 mW typical)**

Features

- Ultra low noise
- Low power
- Fast rise time (2.5 ns at 0 pF)
- External FET (allows selection or cooling)
- Positive or negative signal processing
- Pin selectable gain
- Small size (14 pin hybrid DIP)
- High reliability screening
- One year warranty

Applications

- Aerospace
- Nuclear physics
- Portable instrumentation
- Nuclear monitoring
- Particle, gamma, and x-ray imaging
- Medical and nuclear electronics
- Electro-optical systems

Overview

The A250 is a hybrid state-of-the-art Charge Sensitive Preamplifier for use with a wide range of detectors having capacitance from less than one, to several thousand picofarads. Such detectors include silicon, CdTe, CZT, and HgI_2 solid state detectors, proportional counters, photomultiplier tubes, piezoelectric devices, photodiodes, CCD's, and others.

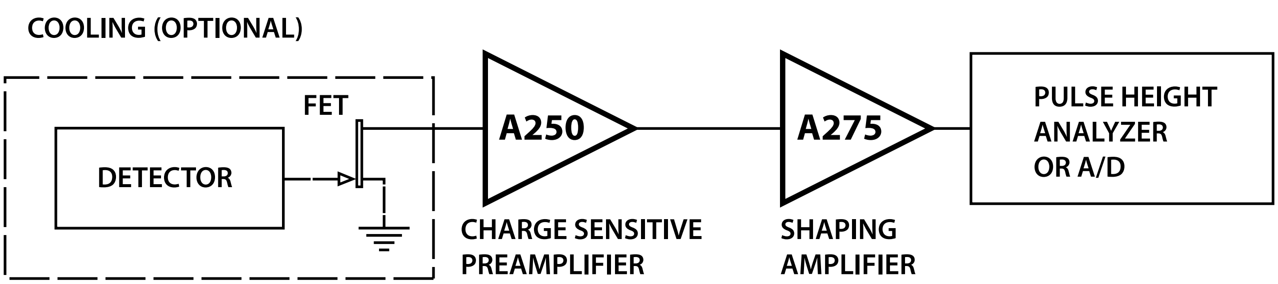
To permit optimization for a wide range of applications, the input field effect transistor is external to the package and user selectable. This feature is essential in applications where detector and FET must be cooled to reduce noise. In all applications, it allows the FET to be matched to the particular detector capacitance, as well as to noise and shaping requirements. In larger quantities, the A250 may be specially ordered with an internal FET.

The noise performance of the A250 is such that its contribution to FET and detector noise is negligible in all charge amplifier applications, i.e., it is essentially an ideal amplifier in this respect.

The internal feedback components configure the A250 as a charge amplifier; however, it may be used as a high performance current or voltage preamplifier by choice of suitable feedback components.

While these preamps were designed for multidetector satellite instrumentation, their unique characteristics make them equally useful in a broad range of laboratory and commercial applications.

Figure 1: Typical Application



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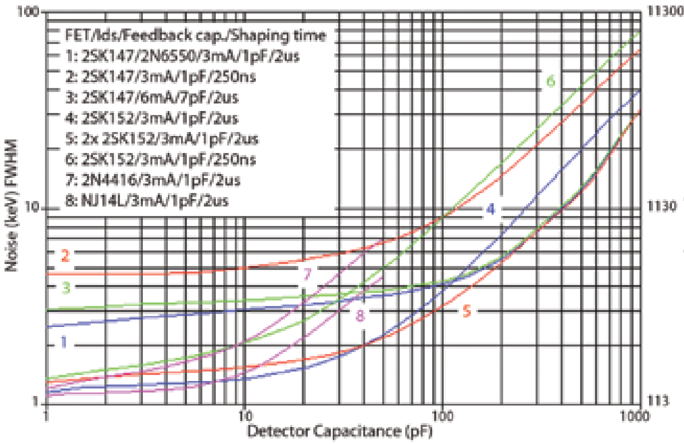
A250 Specifications (V_S = ±6 V, T = 25 °C unloaded output)

INPUT CHARACTERISTICS	
Sensitivity (C_f = 1 pF)	44 mV/MeV (Si) 55 mV/MeV (Ge) 36 mV/MeV (CdTe) 38 mV/MeV (HgI_2) 1 V/pC 0.16 µV/electron
Sensitivity can be reduced by connecting Pin 2 and/or 3 to Pin 1, thus providing C_f = 3, 5, or 7 pF. Additional external capacitors can be added for further reduction of gain. In general, the sensitivity is given by A = 1/C_f (pF) V/pC. For silicon, the sensitivity is A = 44/C_f (pF) mV/MeV.	
Noise	Input FET dependent. See Figure 2.
Noise slope	Input FET dependent. See Figure 2.
Data presented in Figure 2 is representative of results obtained with recommended FETs, and is characteristic of the FET and shaping time constants, rather than the A250, which is effectively noiseless. In general, the choice of input FET is based on its noise voltage specification (ηV/√Hz) and its input capacitance (C_{iss}). For low capacitance detectors, a FET with small C_{iss} should be chosen, such as 2N4416 or 2SK152. For very high capacitance detectors, two or more matched high C_{iss} FETs such as the 2N6550 may be paralleled to achieve the best noise performance.	
Dynamic Input Capacitance	>40,000 pF with two 2SK147 FETs and C_f = 5 pF
Polarity	Negative or positive
OUTPUT CHARACTERISTICS	
Polarity	Inverse of input
Rise Time	2.5 ns at 0 pF input load with 2SK152 4.5 ns at 100 pF input load with 2N6650 or 2SK152. See Figures 3 and 4.
Output Impedance	Pin 8: 100 Ω; Pin 9: < 10 Ω.
Integral Nonlinearity	< 0.03% for 0 to +2 V unloaded < 0.006% for 0 to -2 V unloaded
Decay Time Constant	300 MΩ x C_f = 300 µs, 900 µs, 1.5 ms, 2.1 ms. User selectable T=$R_f C_f$
Positive Clipping Level	> +2.8 V
Negative Clipping Level	< -4.6 V
GENERAL	
Gain-Bandwidth Product	f_T > 300 MHz with 2N4416 FET f_T > 1.5 GHz with two 2SK147 FETs See Figure 7.
Operating Voltage	±6 V, (±8 V maximum)
Operating Current	±1.2 mA plus the FET drain current (I_{ds}). Where: I_{ds} (mA) = 3/R (kΩ) - 0.25. As a special case, the internal 1 K resistor may be used for R, by connecting Pin 13 to 14, giving I_{ds} = 2.75 mA.

Power Dissipation	14 mW + 6[I_{ds}]
Variation of Sensitivity with Supply Voltage	< 0.15%/V at ±6 V.
Temperature Stability	< 0.1% from 0 to +100 °C < 0.5% from -55 to +125 °C
Operating Temperature	-55 to +125 °C
Storage Temperature	-65 to + 150 °C
Screening	Amptek High Reliability
Package	14 Pin hybrid DIP (metal)
Weight	3.8 g
Warranty	One year
Test Board	PC-250
Options	RC Feedback Kit (1 GΩ resistor, 0.1 pF capacitor) Internal FET (consult factory) NASA GSFC S-311-P-698 screening Amptek High Reliability Screening
Other Configurations (Package)	A250F with internal FET (SIP Package) A250F/NF with external FET (SIP Package)
Pin Configuration (14 pin hybrid DIP)	
Pin 1	300 MΩ resistor in parallel with 1 pF feedback capacitor. Connect this pin to the detector and the gate of the FET.
Pin 2	2 pF feedback tap
Pin 3	4 pF feedback tap
Pin 4	-6 V direct
Pin 5	-6 V through 50 Ω
Pin 6	Compensation (0 - 30 pF to ground) for low closed loop gain configuration (where a large feedback capacitor is used together with small detector capacitance).
Pin 7	Ground and case
Pin 8	Output through 100 Ω
Pin 9	Output direct
Pin 10	+6 V through 50 Ω
Pin 11	+6 V direct
Pin 12	Ground and case
Pin 13	Provide 2.75 mA drain current to the external FET by connecting Pin 13 to 14. (See operating current specifications.)
Pin 14	Input. Should be connected to the drain of the FET. This pin is held internally at + 3 Volts.

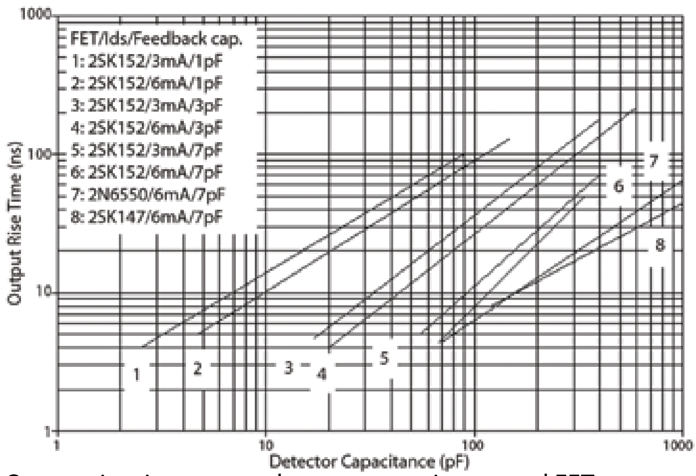
A250 Specifications (con't)

Figure 2: A250 Noise Characteristics



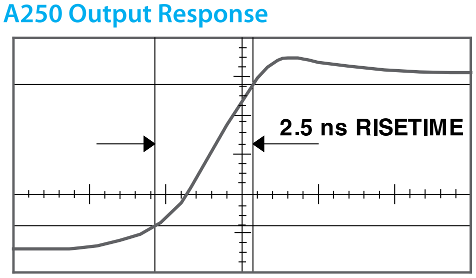
Noise as a function of detector capacitance, input FET, feedback capacitor, and shaping times

Figure 3: A250 Rise Time



Output rise time versus detector capacitance and FET

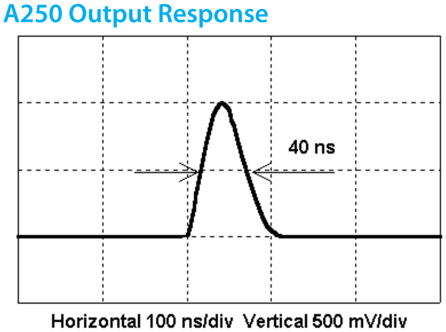
Figure 4: A250 Output Response



Horizontal = 2 ns/div. Vertical = 500 mV/div.

Output response with A250 configured as a charge sensitive preamplifier; 2SK152/3mA, $R_f = 300\ M\Omega$, $C_f = 1$ pF, $C_d = 0$ pF

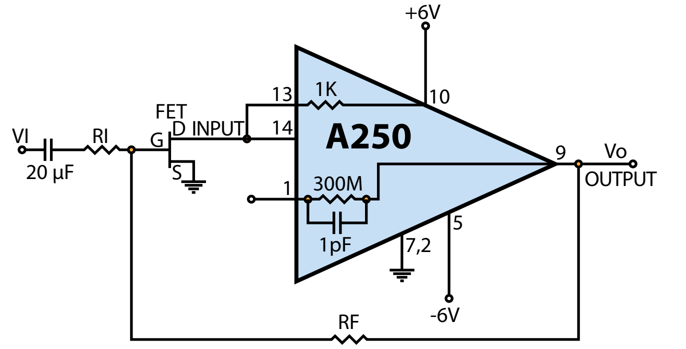
Figure 5: A250 Output Response



Horizontal 100 ns/div Vertical 500 mV/div

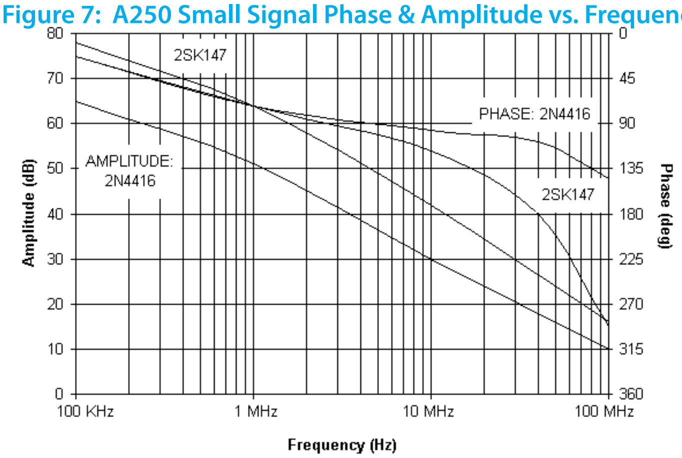
Output response with A250 configured as a Transimpedance Amplifier (current to voltage); 2N4416/3mA, $R_f = 60\ k\Omega$, $C_f = 0$ pF, $C_d = 0$ pF

Figure 6: A250 Configured as a Low Noise Voltage Amplifier



Typical RF = 1M, RI = 10K; GAIN: Vo = VI(RF/RI)

Figure 7: A250 Small Signal Phase & Amplitude vs. Frequency



For low capacitance FET: 2N4416 ($C_{iss} = 4$ pF, $I_{ds} = 3$ mA)
For high capacitance FET: 2 x 2SK147 ($C_{iss} = 180$ pF, $I_{ds} =$ 1.5 mA each)

Figure 8: A250 Connection Diagram

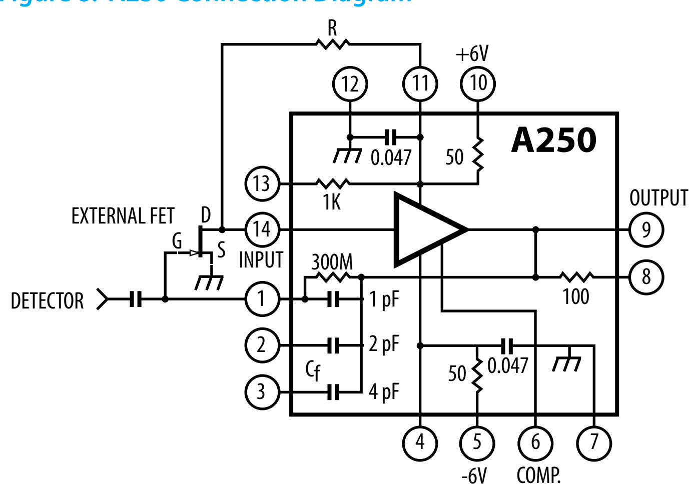


Figure 9: A250 Mechanical dimensions.

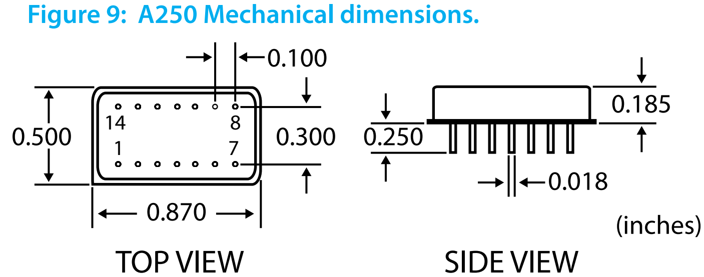


Figure 10: A Two Detector Telescope System.

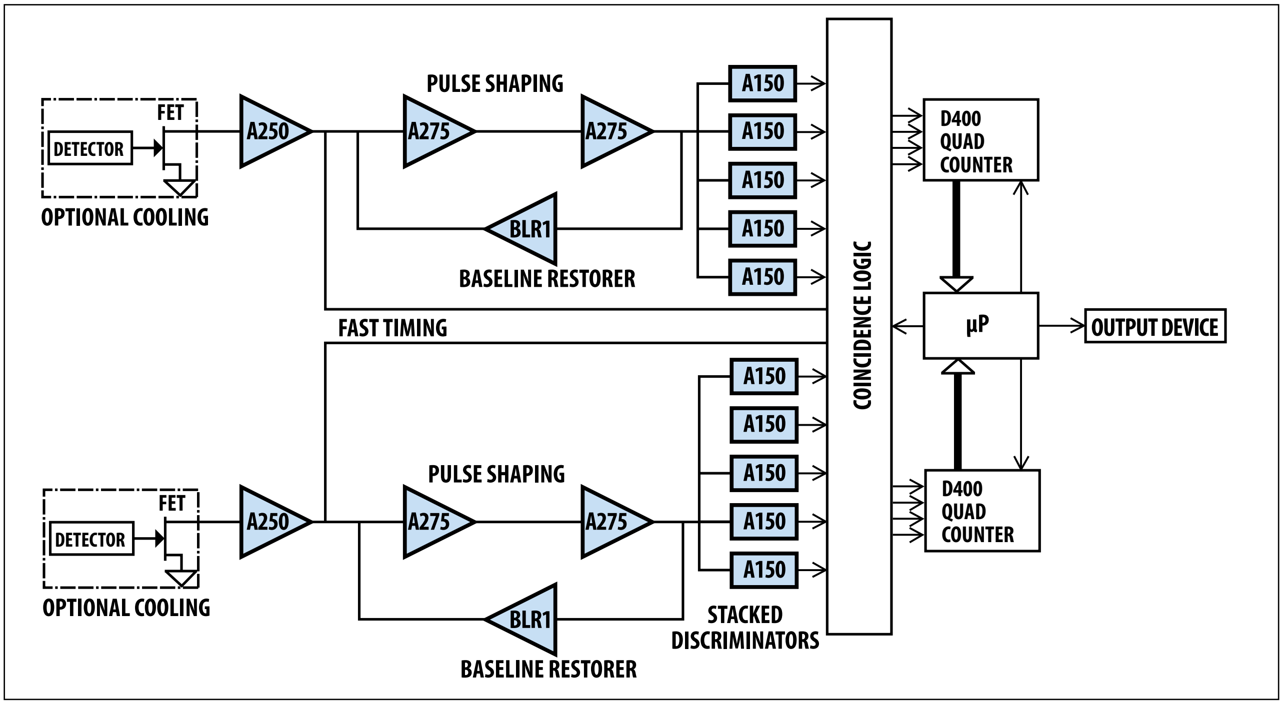


Figure 11: The A250 Connected to a Solid State Detector.

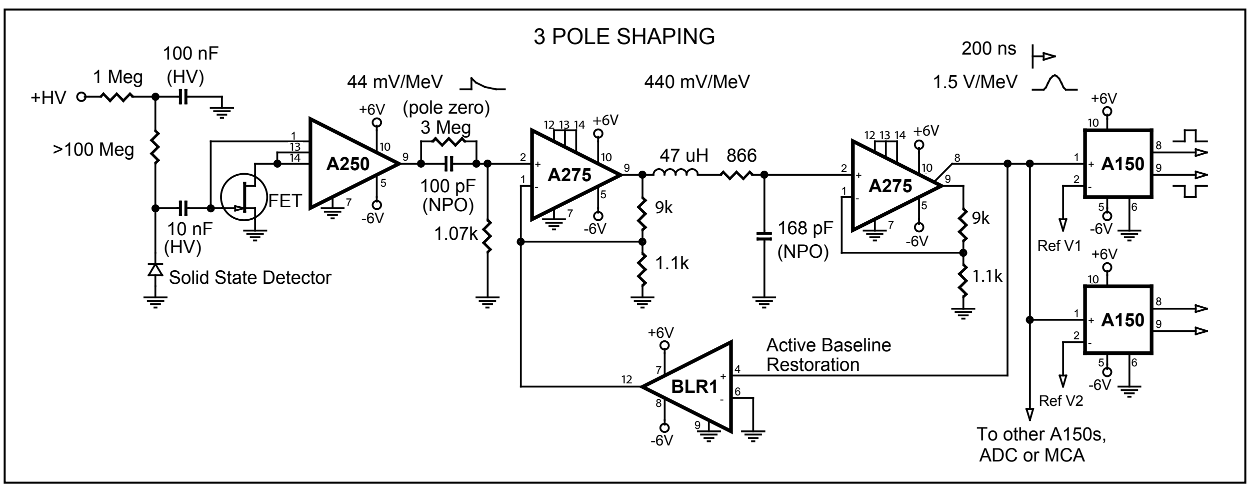


Figure 12: The A250 Connected to a Proportional Counter.

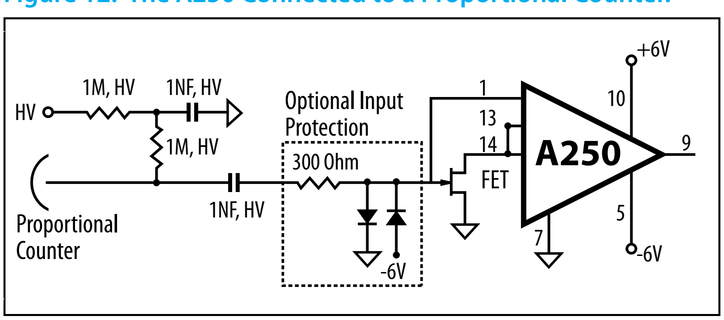
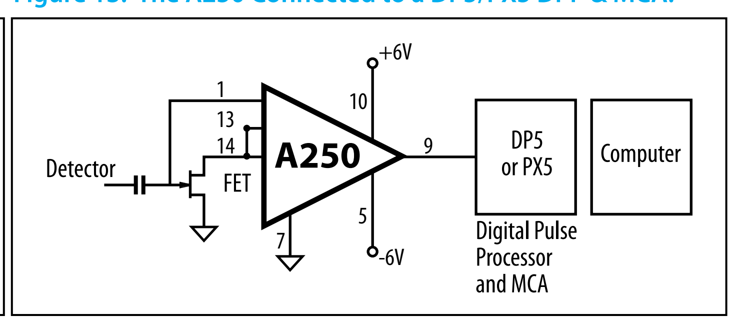


Figure 13: The A250 Connected to a DP5/PX5 DPP & MCA.



For more information, please see http://www.amptek.com

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